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| **FFT** |
| **Students :** Roy Shvadron, Omri Freund  **Supervisor :** Goel Samuel  **Semester :** Winter 2017 |
| **Project Description :**  Diagnostic ultrasound has been used for decades to visualize body structures. As we all probably know, the ultrasound machines are of great size, cost and power consumption. SAMPL lab results prove that using Sub-Nyquist sampling can port the heavy computational tasks to the cloud is feasible for medical ultrasound, leading to potential of considerable reduction in future ultrasound machines size, power consumption and cost. The mixed signal solution of the ultrasound cloud processing includes an ASIC which is comprised of Buffer 🡪 Mixer 🡪 Digital LPF 🡪 buffer 🡪 FFT engine 🡪 buffer.    The goal of this project is to implement the second half of the signal path :  Buffer 🡪 FFT engine 🡪 buffer. The implementation should include an efficient VLSI architecture for the FFT engine. |

**Project Specifications:**

* Clock Frequency : 100 MHz
* Area : 6x6 sq. mm
* Technology : Tower CMOS 180 nm

**Project Requirements:**

* Efficient architecture
* Meeting timing requirements
* Maximum silicon area efficiency
* Minimal output error
* Synthesis
* Physical design (layout)

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| **Development Stages / Design Flow** | **Tools** |
| Software Simulation | Matlab |
| Architectural and Logic Design |  |
| HDL Implementation | Verilog |
| Functional simulation | Ncsim/VCS |
| Synthesis | Design Compiler |
| Layout Design | First Encounter |

**Literature:**

**Work in progress**

**Alternative solutions:**

**Work in progress**

**Selected solution :**

**Work in progress**

**Top Level Interface:**

**Work in progress**

**Top Level Architecture:**

**Work in progress**

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| **Provisional/Preliminary Schedule**  Matlab simulations in order to calculate  the registers length  Architectural and logic design  Implement the Architecture using Verilog  Functional simulation  Layout Design   Report | **Week**  1-3  4-6  7-8  9-10  11-12  13-14 |

Week 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Matlab Simulation

Architectural and Logic Design

Verilog Implementation

Functional simulation

Synthesis

Layout Design

Report